



# Togo Capacitor Calibration Company

Introduction. Successive approximation register (SAR) analogue-to-digital converters (ADCs) with mainly digital circuits and simple analogue circuits have been widely used in medium-resolution and medium-speed applications, such as environmental monitoring, battery monitoring, and motor control [1-5]. However, capacitor mismatch is a major factor that limits ...

calibration is of the direct null type, and the capacitor calibration is of the comparative null type. In other words, the accuracy of the capacitance measurements ultimately depends on the uncertainty in assigning a value to a standard capacitor. The stan

These high precision calibration capacitors come with excellent insulation. In combination with a precise voltage source, charge signals may be generated as needed. The family Type 5371A is ...

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In Fig. 1, during the foreground calibration phase, the capacitor recombination digital module receives the output of the comparator during the capacitors comparison and obtains the sorting results of capacitors size. During the normal conversion phase, the SAR logic control module controls the optimal capacitor after capacitor recombination by controlling ...

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This paper presents a foreground calibration algorithm combination with a background calibration algorithm for successive approximation register analog-to-digital converters (ADC). The foreground calibration for capacitor mismatch is capacitor recombination algorithm and the background calibration for capacitor mismatch is single-channel least mean ...

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An efficient two-phase calibration technique for 1-bit/stage pipelined Analog-to-Digital Converters (ADCs) is



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presented in this paper. The proposed technique employs linear histogram testing to collect the required information to calibrate the non-ideal ADC output behavior induced by capacitor mismatch and comparator offset. In the first phase, it calibrates ...

Fig. 3 Proposed capacitor mismatches calibration before calibration after calibration ENOB, bits 4 bit improvement mismatch error, % 10-2 14 13 12 11 10 9 10-3 Fig. 4 Monte Carlo simulation with added capacitor mismatches in split-CDAC Capacitor mismatch calibration: Fig. 3 presents the proposed capacitor mismatch calibration logics.

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This paper presents a high-resolution 18-bit SAR ADC with a high 10-bit capacitor DAC and a low 8-bit resistor DAC. The total required number of the unit capacitors is decreased to 512. Foreground digital calibration based on capacitive recombination is introduced to improve linearity. Preamplifiers and output offset storage(OOS) enhance the noise and offset ...

A novel digital calibration technique is proposed to calibrate the capacitor mismatch in SAR ADCs. The capacitor mismatches are extracted based on the comparator metastability and intrinsic noise. The proposed technique does not require additional external control sequences or any modification of the main DAC. The simulation results of a 12-bit SAR ADC with 10% capacitor ...

To address the capacitance array mismatch in SAR ADCs, this paper proposes a novel capacitor calibration scheme based on the Time-to-Digital Converter (TDC). This scheme achieves calibration accuracy as high as 0.01% ...

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match in SAR ADCs, this paper proposes a novel capacitor calibration scheme based on the Time-to-Digital Converter (TDC). This scheme achieves calibration accuracy as high as 0.01% and can be flexibly de-signed to meet the accuracy requirements of SAR ADCs. Simulation results indicate that the capacitance mismatch issue of a redundant ca-

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